APPENDIX A

A.1 INTRODUCTION This appendix was developed by the IPC 1-10c Test Coupon and Artwork Generation Task Group and is included in this current document revision as a resource for the design of conformance and qualification coupons. The intent is to provide guidance as to the coupon designs, however if conflicts arise or the information provided is incomplete, the design of the coupon features should be in accordance with the associated product board design requirements.

It is the task group's recommendation that the coupons be designed by the printed board fabricator in order to ensure that the correct drill sizes are used. Additionally, etch and solder mask fabrication compensation **shall** be applied uniformly to both the coupons and product board after the coupons have been designed.

Solder mask layers are documented for each of the coupons, however they are only to be used if the associated product board design requires solder mask.

Table A.1-1 provides a summary of coupon designs that are described within this appendix.

Table A.1-1 IPC Coupons

Section	Coupon	Description	Purpose
A.2	AB/R	General purpose AB coupon for through features	Plated hole/via evaluation, feature size and spacing, registration, thermal stress and rework simulation
A.3	A/R	General purpose A coupon for use when B features are not present	Plated hole evaluation, feature size and spacing, registration, thermal stress and rework simulation
A.4	B/R	B coupon for non-through (propagated) via features	Plated hole evaluation, registration and thermal stress
A.5	E	Moisture and insulation resistance coupon	Moisture and insulation resistance
A.6	S	Hole solderability coupon	Hole solderability
A.7	W	Surface mount solderability coupon	Surface mount solderability
A.8	D	General purpose AB daisy-chain via coupon	Plated hole/via thermal stress
A.9	G	Solder mask coupon	Solder mask adhesion
A.10	H	Surface insulation resistance coupon	Surface insulation resistance
A.11	P	Peel strength coupon	Peel strength and plating adhesion
A.12	Z	Controlled impedance coupon	Controlled impedance

A.2 AB/R COUPON Coupon AB/R combines the heritage A, B and R coupon design features along with a C feature which represents the smallest via or component hole which has the smallest annular ring. In order to better represent the product board the B1 feature contains internal lands only on layers 2 and n-1, the B2 feature contains lands only on internal signal layers and the B3 feature contains internal lands only on plane layers. The design also includes features to allow the assessment of minimum conductor and space widths from the product board. To accomplish this, the B4 lands are square and the minimum conductor for each layer is located adjacent to the B4 lands at the minimum spacing for each layer.

The R feature provides a method to electrically assess 360° registration without the need for microsectioning. Due to the contribution of etch variation with heavier innerlayer foils use of the R features is recommended for design with foil weights of 1 oz. or less. The design parameters for coupon AB/R are shown in Table A.2-1.

Table A.2-1 AB/R Coupon Parameters, mm [in]

<table>
<tr><th>Feature</th><th>Description</th><th>Design Requirements</th></tr>
<tr><td>A</td><td>Largest component hole with its smallest associated D+
Round lands on all layers</td><td>Drill size shall be ≤1.07 [0.042]
Land size shall be ≤1.65 [0.065]</td></tr>
<tr><td>B1</td><td>Smallest via with its smallest associated D+ Round lands on layers 2 and n-1</td><td rowspan="4">Land size shall be ≤1.02 [0.040]
Grid size: 1.27 [0.050]</td></tr>
<tr><td>B2</td><td>Smallest via with its smallest associated D+ Round lands on signal layers</td></tr>
<tr><td>B3</td><td>Smallest via with its smallest associated D+ Round lands on plane layers</td></tr>
<tr><td>B4</td><td>Smallest via with its smallest associated D+ Square lands on all layers</td></tr>
<tr><td>C</td><td>Smallest D+ with its smallest associated via or component hole
Round lands on all layers</td><td>Drill size shall be ≤1.07 [0.042]
Land size shall be ≤1.65 [0.065]</td></tr>
<tr><td>RA</td><td>Registration based on the A feature</td><td rowspan="3">Anti-land calculation (minimum of):
(Land diameter + 0.0127 [0.0005]) - (2 x annular ring requirement)
or
(Drill diameter + 2 x minimum edge of hole-to-copper spacing + 0.0127 [0.0005]) - (2 x minimum copper-to-copper spacing requirement)</td></tr>
<tr><td>RB</td><td>Registration based on the B feature</td></tr>
<tr><td>RC</td><td>Registration based on the C feature</td></tr>
<tr><td>RB1</td><td>Registration based on the B feature with a 0.0254 [1.0] allowance</td><td>Anti-land calculation:
RB anti-land + 0.0508 [0.002]</td></tr>
<tr><td>G</td><td>Common connection for “R” measurements</td><td>Maximum drill size is 0.51 [0.020]
Land size is 1.02 [0.040]</td></tr>
<tr><td>L</td><td>Minimum conductor width (in line with B4 lands)</td><td>Minimum conductor for each layer</td></tr>
<tr><td>S</td><td>Minimum space width (in line with B4 lands)</td><td>Minimum space for each layer</td></tr>
<tr><td>T</td><td>Tooling hole</td><td>Drill size is 2.00 [0.0787]</td></tr>
</table>

Note 1. Thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. The “R” measurements should be used with caution for copper weights greater than 1 oz. or when positive etchback greater than 0.0127 [0.0005] is present.
Note 3. For direct plane layer connections B3 and B4 pad size are 1.02 [0.040].
Note 4. B1, B2 and B3 **shall** have lands on every layer for designs using non-functional lands.
Note 5. When the smallest B land exceeds 1.02 [0.040], a modified A/R coupon with a unique designation (e.g., A/R-1) **shall** be used to assess the via feature. Complete documentation of this new coupon and its design requirements will be provided in a subsequent revision to this Appendix.

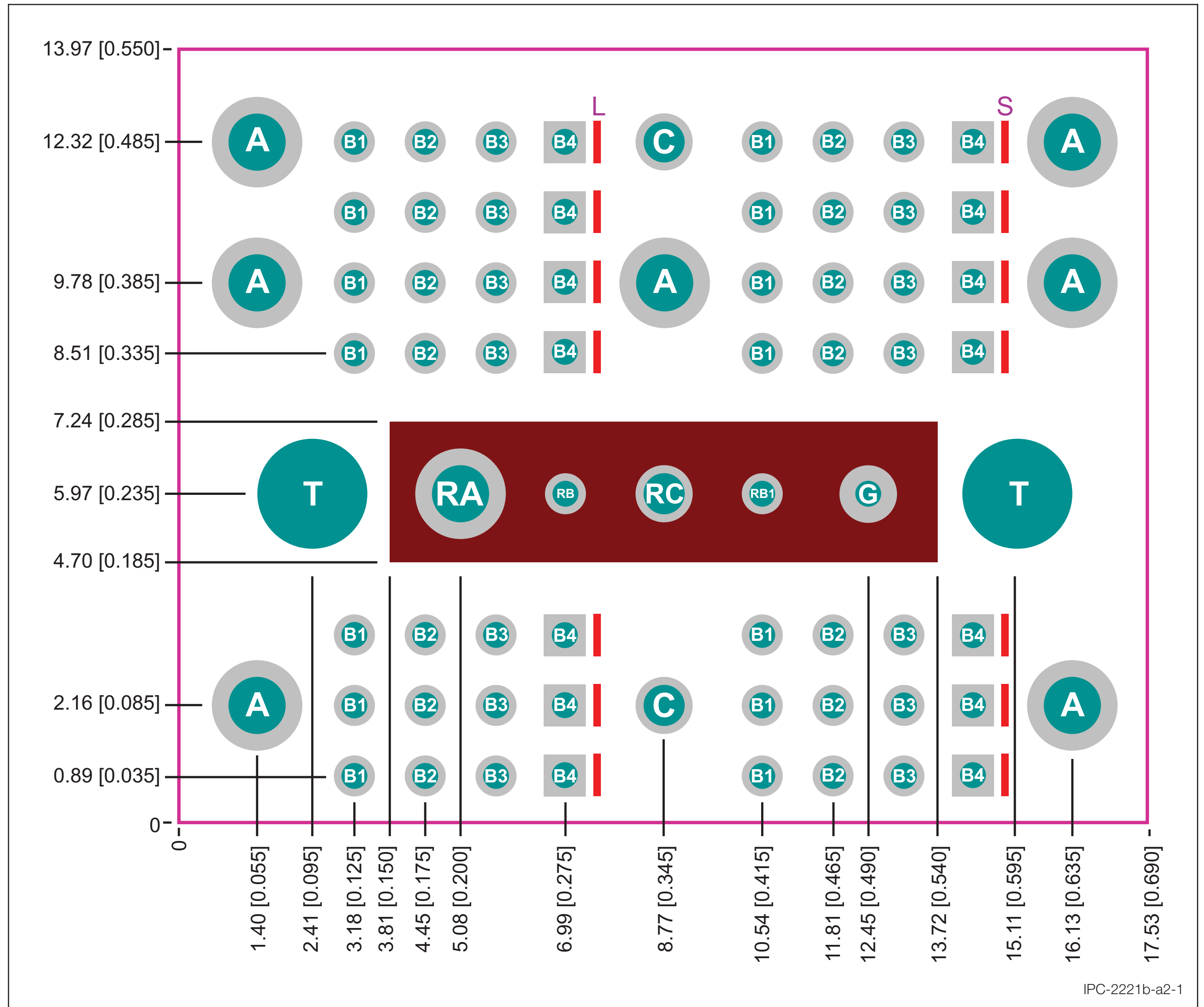

Figure A.2-1 AB/R Coupon Layout, mm [in]

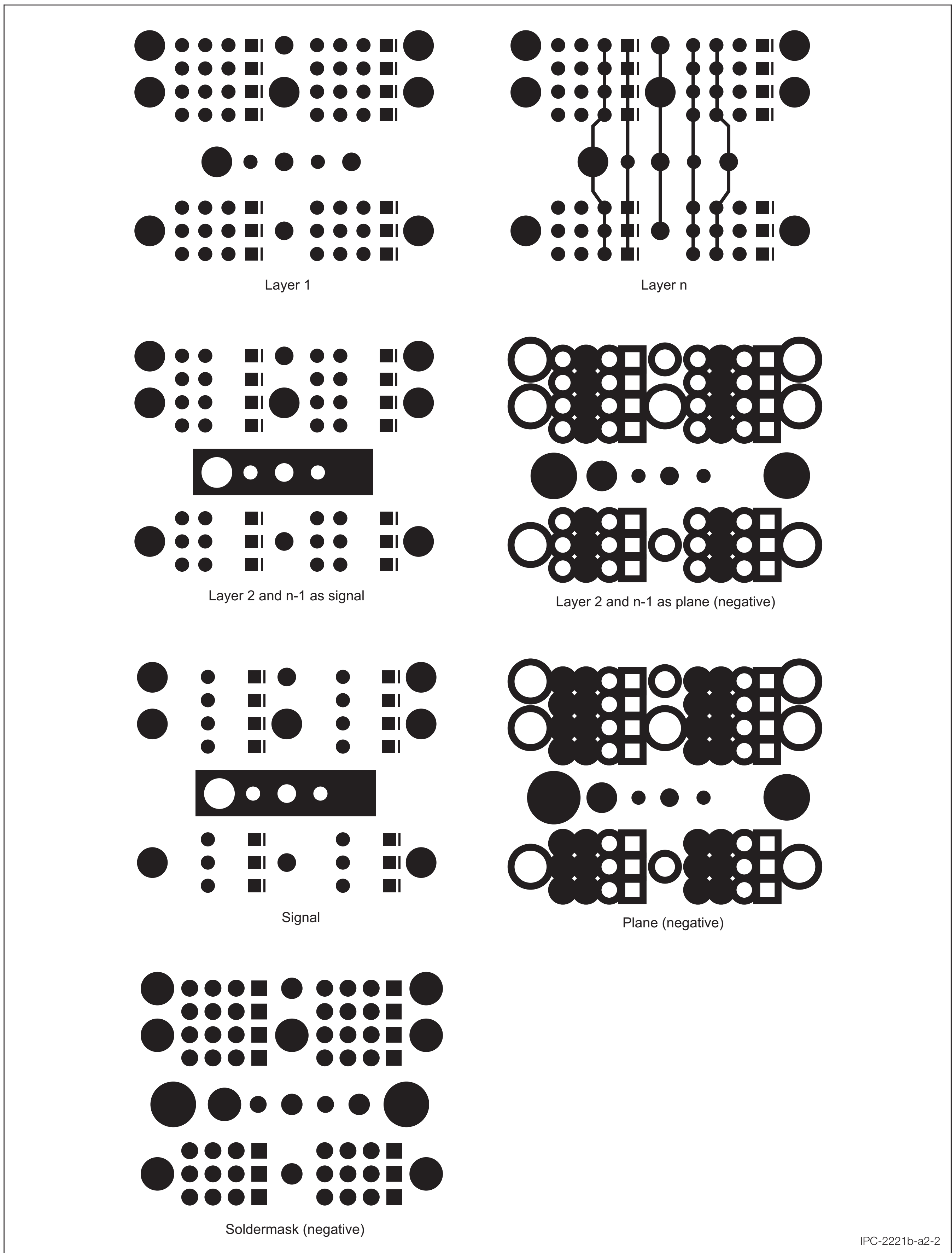

Figure A.2-2 AB/R Coupon Example Layers

A.3 A/R COUPON Coupon A/R follows the same design intent as the AB/R except that it is intended for use when the product board does not contain any vias. The design parameters for coupon A/R are shown in Table A.3-1.

Table A.3-1 A/R Coupon Parameters, mm [in]

Feature	Description	Design Requirements
A1	Largest component hole with its smallest associated D+ Round lands on layers 2 and n-1	Drill size **shall** be ≤1.07 [0.042] Land size **shall** be ≤1.65 [0.065] Grid: 1.91 [0.075]
A2	Largest component hole with its smallest associated D+ Round lands on signal layers	
A3	Largest component hole with its smallest associated D+ Round lands on plane layers	
A4	Largest component hole with its smallest associated D+ Square lands on all layers	
RA	Registration based on the A feature	Anti-land calculation (minimum of): (Land diameter + 0.0127 [0.0005]) - (2 x annular ring requirement) or (Drill diameter + 2 x minimum edge of hole-to-copper spacing + 0.0127 [0.0005]) - (2 x minimum copper-to-copper spacing requirement)
RA1	Registration based on the A feature with a 0.0254 [1.0] allowance	Anti-land calculation: RA anti-land + 0.0508 [0.002]
G	Common connection for “R” measurements	Maximum drill size is 0.51 [0.020] Land size is 1.02 [0.040]
L	Minimum conductor width (in line with B4 lands)	Minimum conductor for each layer
S	Minimum space width (in line with B4 lands)	Minimum space for each layer
T	Tooling hole	Drill size is 2.00 [0.0787]

Note 1. Thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. The “R” measurements should be used with caution for copper weights greater than 1 oz. or when positive etchback greater than 0.0127 [0.0005] is present.
Note 3. For direct plane layer connections A3 and A4 pad size are 1.65 [0.065].
Note 4. A1, A2 and A3 **shall** have lands on every layer for designs using non-functional lands.

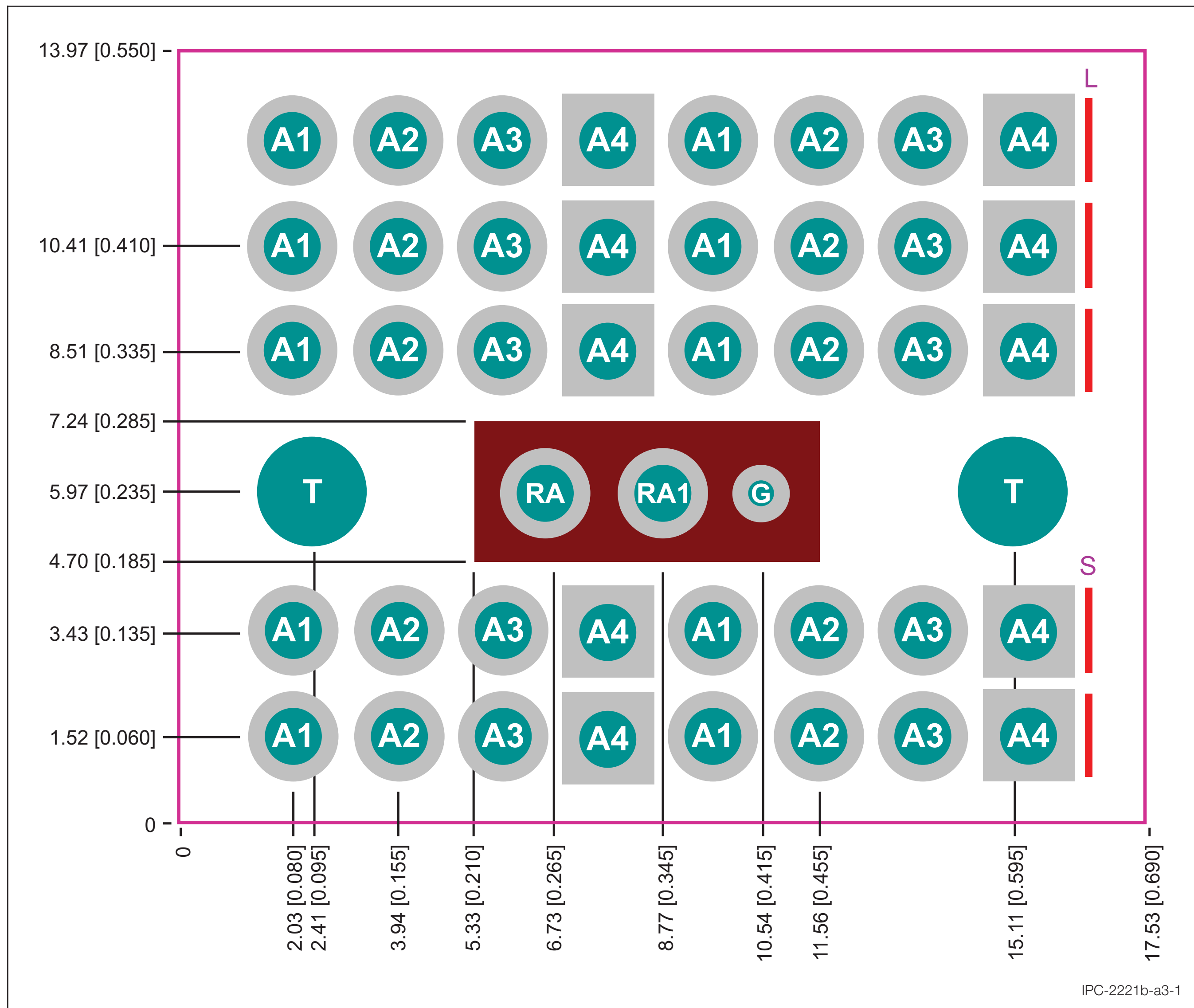

Figure A.3-1 A/R Coupon Layout, mm [in]

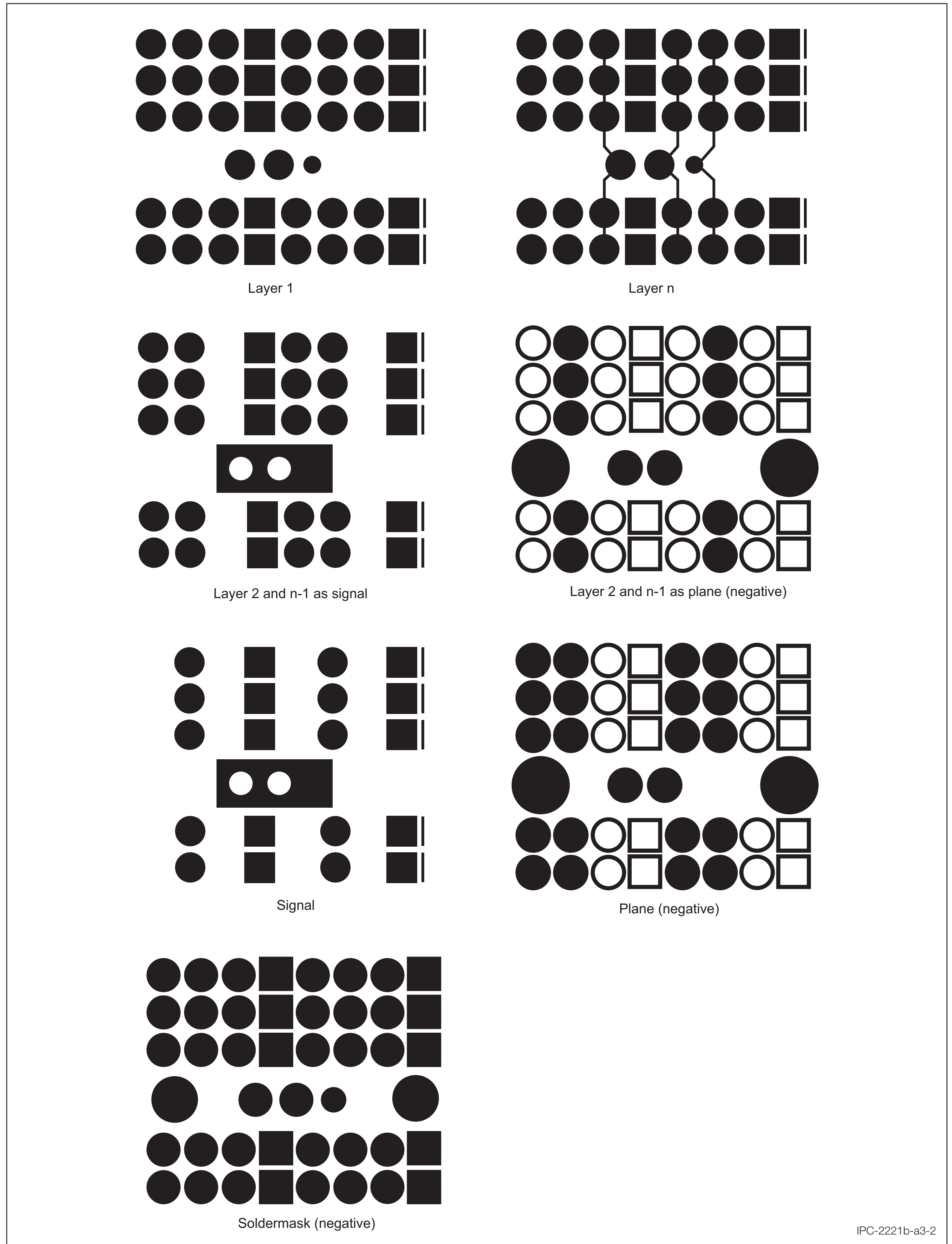

Figure A.3-2 A/R Coupon Example Layers

A.4 B/R COUPON Coupon B/R follows the same design intent as the AB/R except that it is intended for uses with non-through (propagated) via structures. The design provides the opportunity to add up to three different propagated via structures per coupon. The pitch of the B/R design in this Appendix does not support microvia stacked on buried via structures. In the case of microvias the design provides nine holes, each offset in alignment by 0.00635 mm [0.00025 in] to improve the probability of meeting the 10% via diameter requirement during microsectioning. The design parameters for coupon B/R are shown in Table A.4-1.

Table A.4-1 B/R Coupon Parameters, mm [in]

Feature	Description	Design Requirements
BX	Smallest via of type “X” with its smallest associated D+ Round lands on representative layers	Land size **shall** be ≤1.02 [0.040] Grid size: 1.27 [0.050] or Land size **shall** be ≤0.31 [0.012] X grid size: 0.38 [0.015] Y grid size: 0.00635 [0.00025]
BY	Smallest via of type “Y” with its smallest associated D+ Round lands on representative layers	
BZ	Smallest via of type “Z” with its smallest associated D+ Round lands on representative layers	
RBX RBY RBZ	Registration based on the BX, BY and BZ features **Note:** Only applicable to sub-composite via structures which span 3 or more layers	Anti-land calculation (minimum of): (Land diameter + 0.0127 [0.0005]) - (2 x annular ring requirement) or (Drill diameter + 2 x minimum edge of hole-to-copper spacing + 0.0127 [0.0005]) - (2 x minimum copper-to-copper spacing requirement)
G	Common connection for “R” measurements	Maximum drill size is 0.51 [0.020] Land size is 1.02 [0.040]
T	Tooling hole	Drill size is 2.00 [0.0787]

Note 1. Internal or external thieving may be added to the coupon provided it is in accordance with the associated product board design.
Note 2. The “R” measurements should be used with caution for copper weights greater than 1 oz. or when positive etchback greater than 0.0127 [0.0005] is present.
Note 3. BX, BY, and BZ **shall** have lands on every layer for designs using non-functional lands.

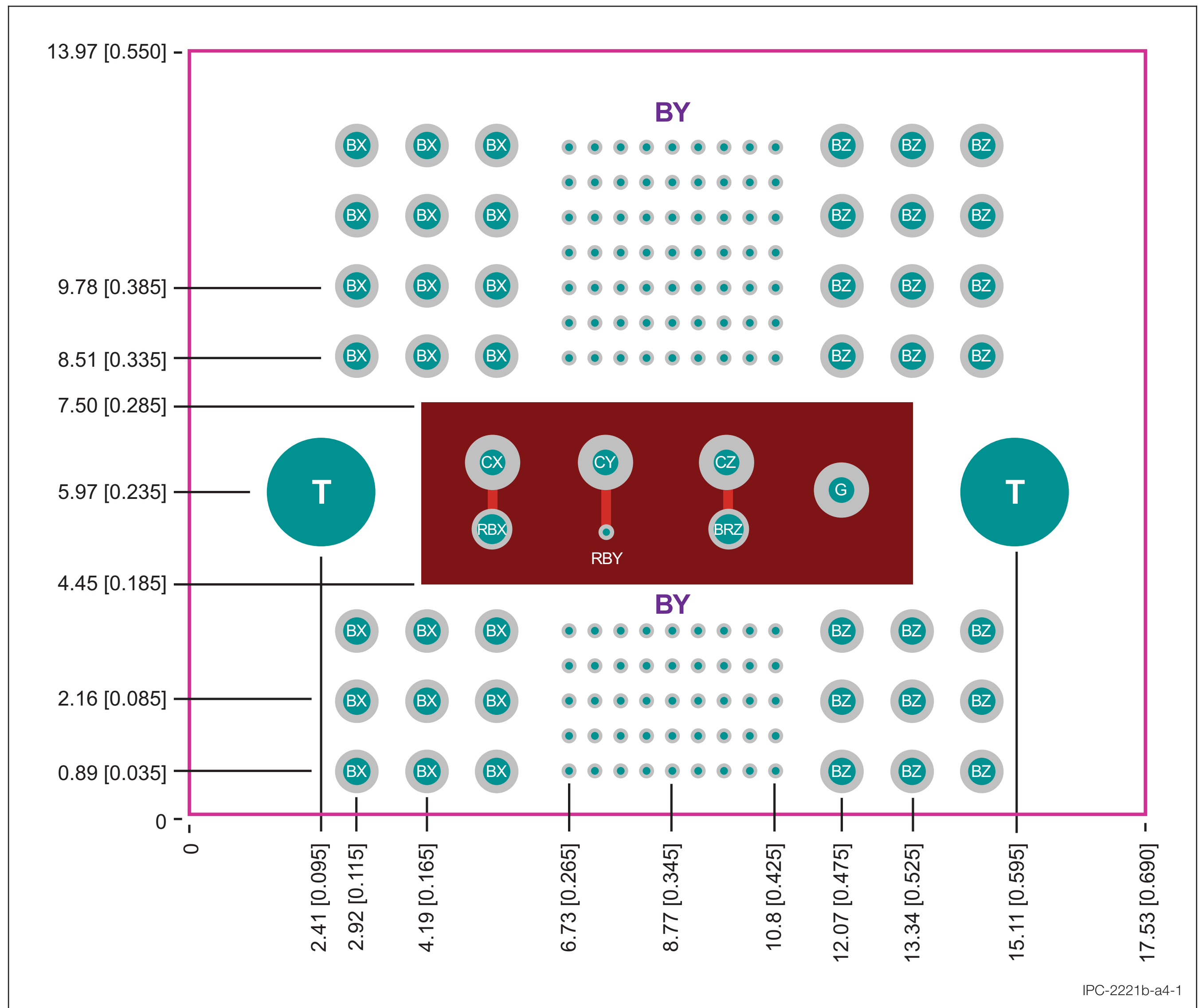

Figure A.4-1 B/R Coupon Layout, mm [in]

A.5 E COUPON Coupon E is used to evaluate moisture and insulation resistance of laminated base materials. The coupon is designed to test a maximum of ten layers. For designs with more than 10 layers additional coupons are required and each **shall** contain the last layer of the preceding coupon (e.g., L1 - 10, L10 - 19, L19 - 28, etc.). The design parameters for coupon E are shown in Table A.5-1.

Table A.5-1 E Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1 - 10	Plated-through test points	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060] Grid: 2.54 [0.100]
Electrodes	Parallel electrodes	Width: 0.635 [0.025] Length: 25.40 [1.000] Gap width: 0.635 [0.025] Plane clearance: 0.635 [0.025]

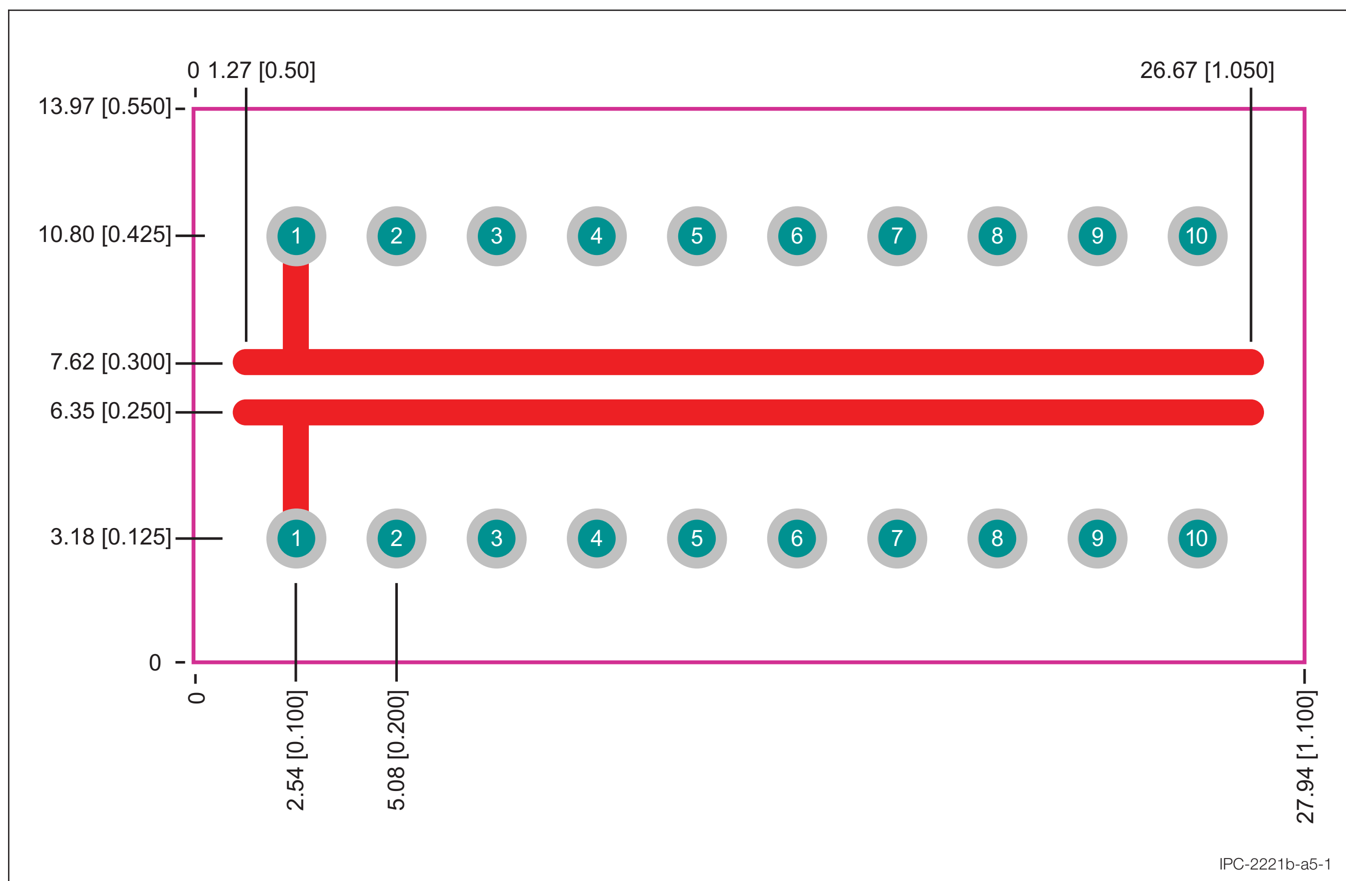

Figure A.5-1 E Coupon Layout, mm [in]

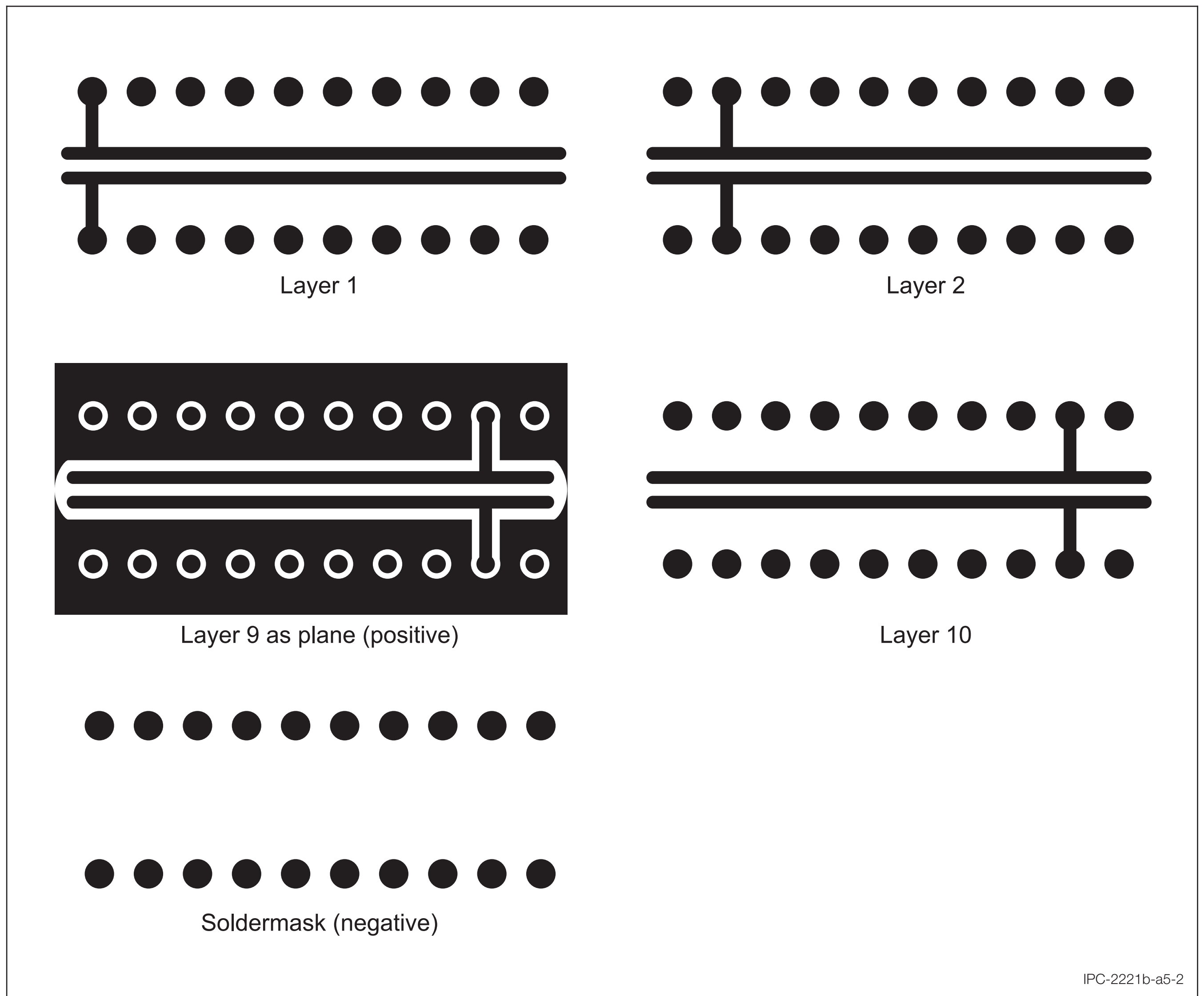

Figure A.5-2 E Coupon

A.6 S COUPON Coupon S is used to evaluate through hole solderability. No innerlayer lands are to be included in the design coupon. The design parameters for coupon S are shown in Table A.6-1.

Table A.6-1 S Coupon Parameters, mm [in]

Feature	Description	Design Requirements
S	Plated-through holes (32 each)	Drill size: 0.81 [0.032] Recommended land size: 1.52 [0.060] Grid: Staggered (see Figure A.6-1)

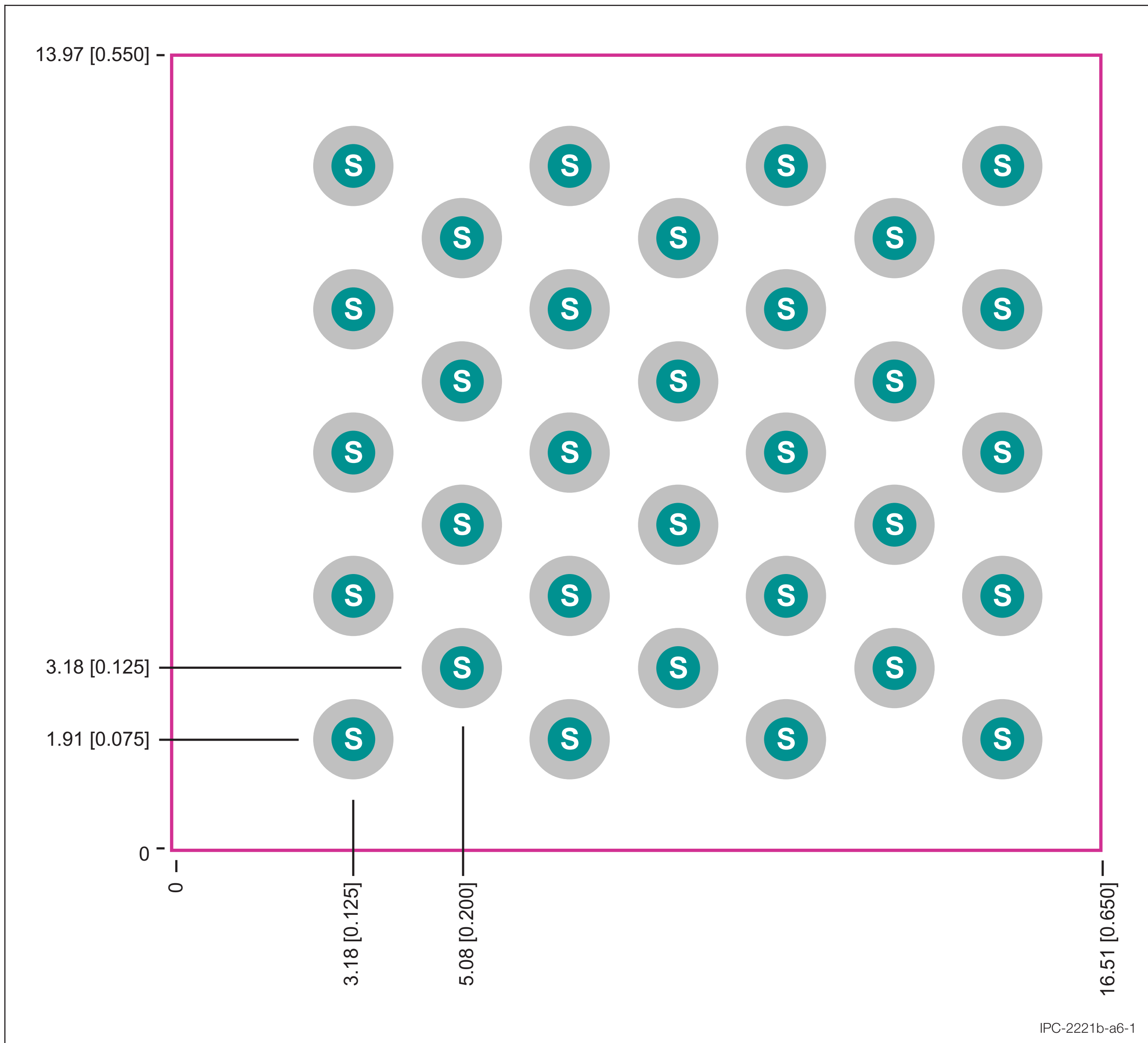

Figure A.6-1 S Coupon Layout, mm [in]

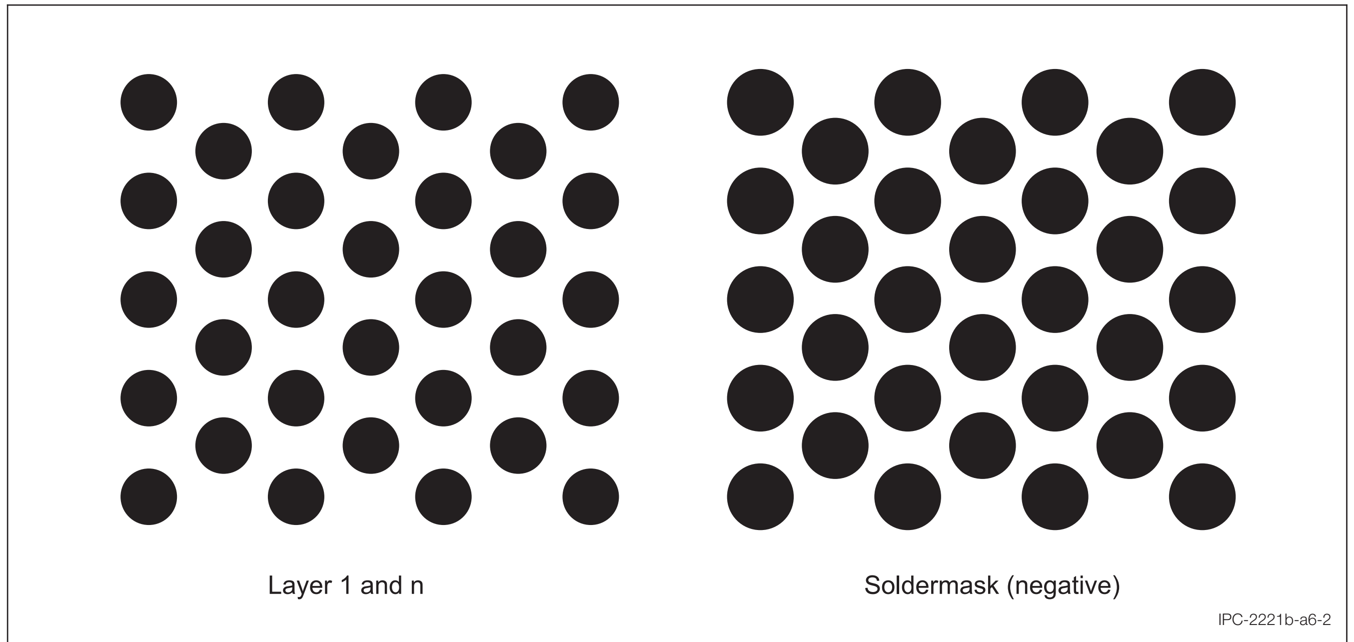

Figure A.6-2 S Coupon Example Layers

A.7 W COUPON Coupon W is used to evaluate surface mount land solderability. By intent, no innerlayers or via structures are included. The design parameters for coupon W are shown in Table A.7-1.

Table A.7-1 W Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Round surface mount lands (7 each)	Land size: 1.52 [0.060] Drill Size: 0.81 [0.032] Pitch: 1.91 [0.075] Solder mask clearance: 0.152 [0.006] greater than land
2	Rectangular surface mount lands (7 each)	Land size: 4.45 x 1.52 [0.175 x 0.060] Pitch: 1.91 [0.075] Solder mask clearance: 0.152 [0.006] greater than land
3	Rectangular surface mount lands (22 each)	Land size: 2.00 x 0.50 [0.079 x 0.020] Pitch: 0.81 [0.032] Solder mask clearance: 0.152 [0.006] greater than land

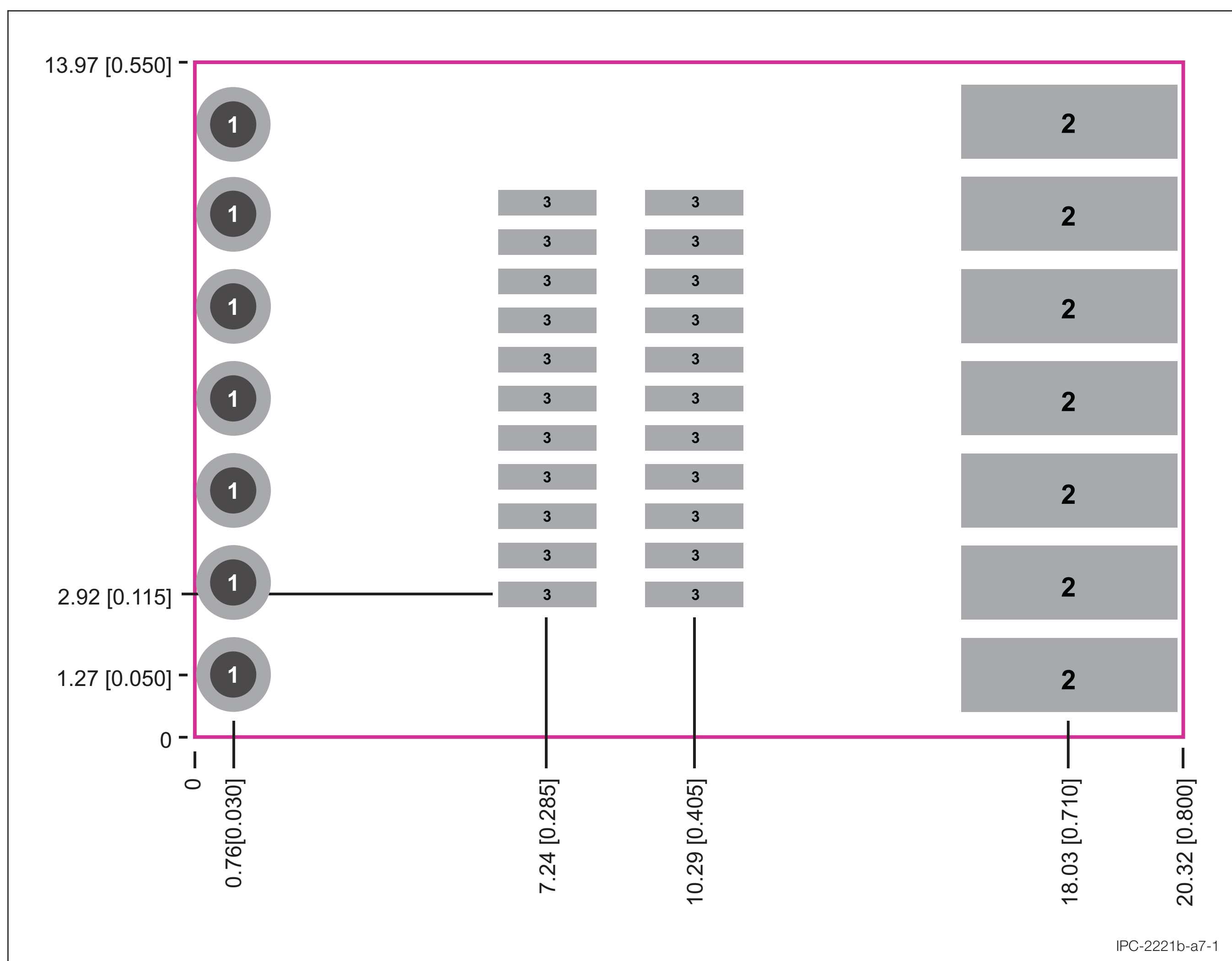

Figure A.7-1 W Coupon Layout, mm [in]

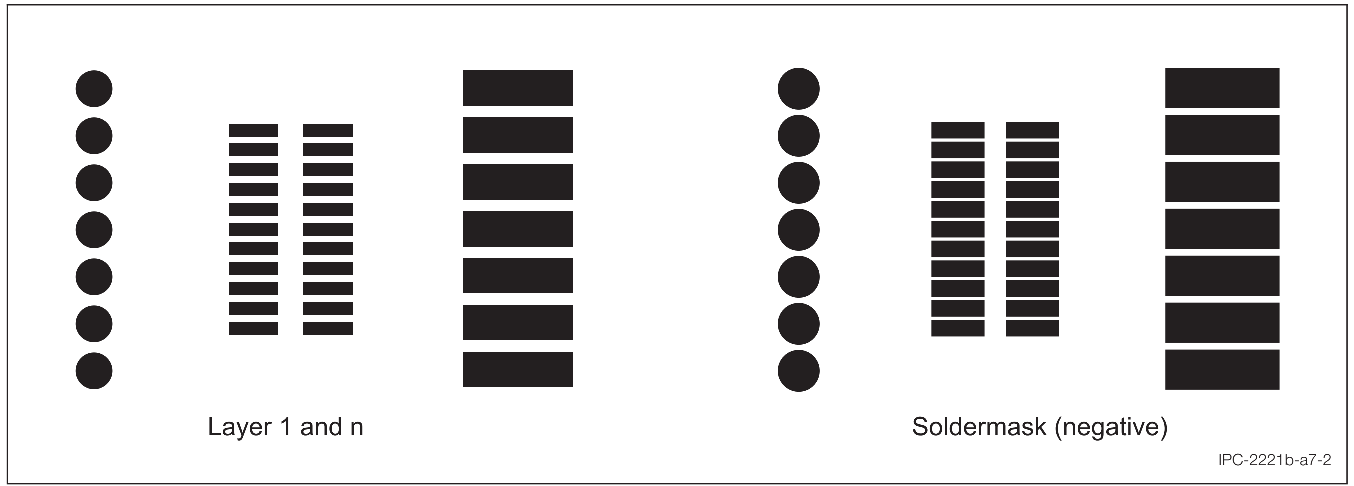

Figure A.7-2 W Coupon Layout

A.8 D COUPON Coupon D is used to evaluate plated hole and via reliability by thermal stress. The coupon is designed to have a sufficient number of plated holes or vias in a chain to obtain precision resistance measurement. The coupon may also be used for propagated via structures as described in Section A.4 by replacing the A and B features with the required propagated via features. The design parameters for coupon D are shown in Table A.8-1.

Table A.8-1 D Coupon Parameters, mm [in]

Feature	Description	Design Requirements
A	Largest component hole with its smallest associated D+ Round lands on layers 2 and n-1	Drill size **shall** be ≤1.07 [0.042] Land size **shall** be ≤1.65 [0.065] Grid: 1.91 [0.075] Interconnect conductors: 0.254 [0.010] Interconnect sequence: Layer 2 to n-1
B	Smallest via with its smallest associated D+ Round lands on layers 2 and n-1	Land size **shall** be ≤1.02 [0.040] Grid size: 1.27 [0.050] Interconnect conductors: 0.254 [0.010] Interconnect sequence: Layer 2 to n-1
Connector	VH: Four-wire resistance high voltage input IH: Four-wire resistance current source VL: Four-wire resistance low voltage input IL: Four-wire resistance current sink	Finished hole size: 1.02 ± 0.076 [0.040 ± 0.003] Land size: 1.91 [0.075] Grid size: 2.54 [0.100] Interconnect conductors: 0.254 [0.010] on Layer 1

Note 1. Each of the chains **shall** contain only one unique via structure.

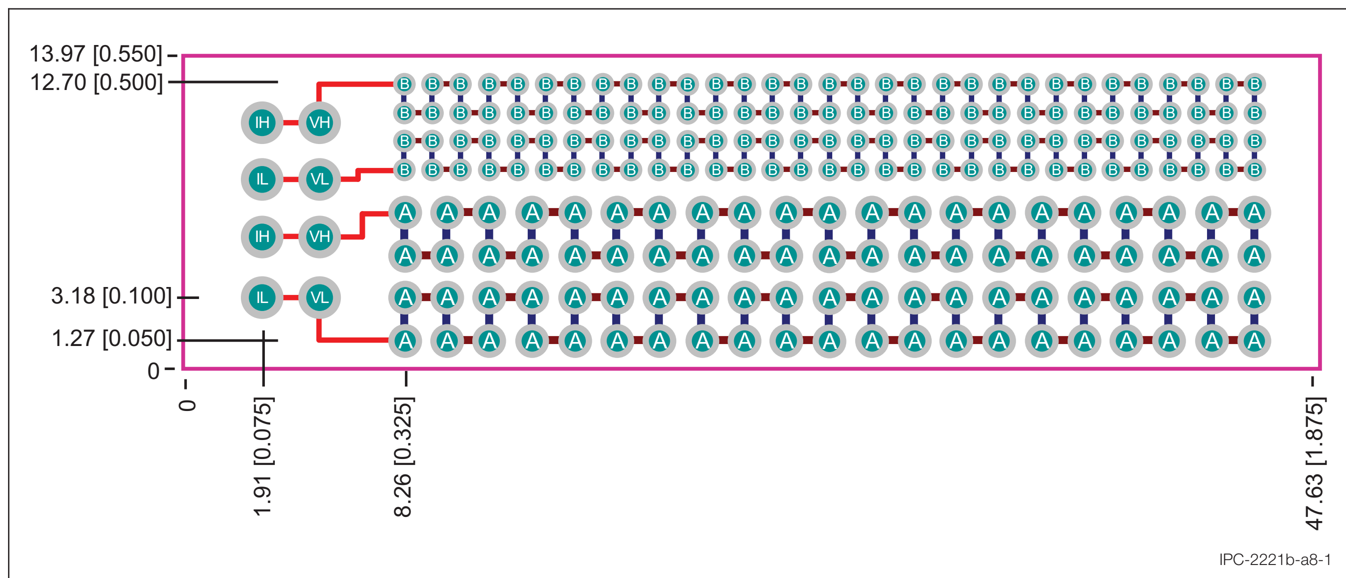

Figure A.8-1 D Coupon Layout with A and B Features, mm [in]

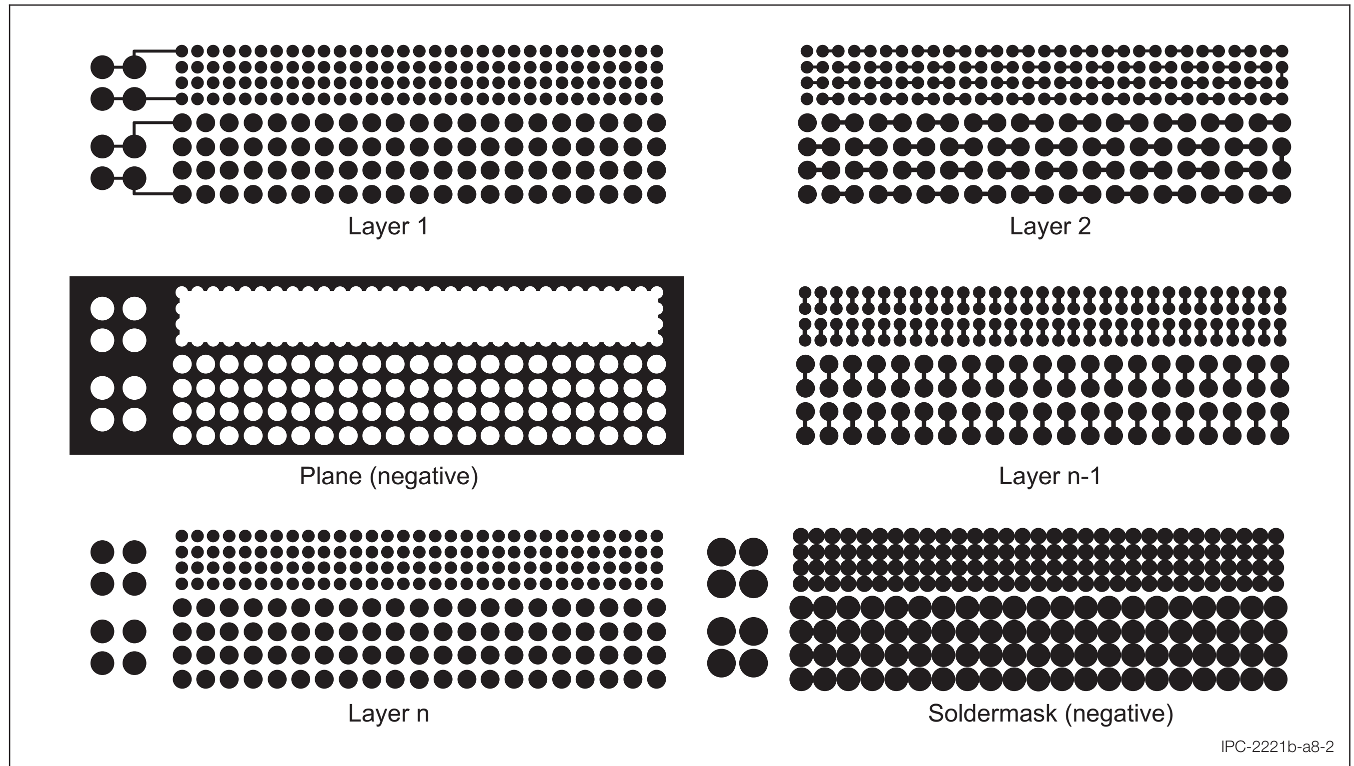

Figure A.8-2 D Coupon Example Layers with A and B Features

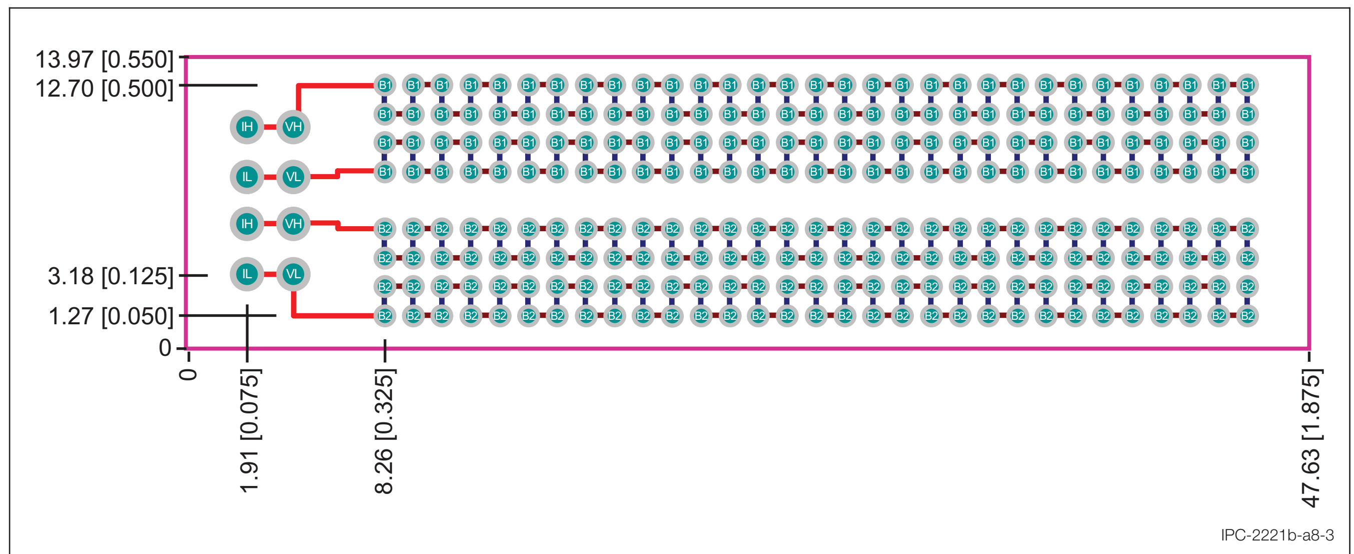

Figure A.8-3 D Coupon Layout with Non-through Via B Features, mm [in]

A.9 G COUPON Coupon G is used to evaluate solder mask adhesion and is divided into three regions 1) solder mask over copper or surface finish, 2) solder mask over laminate and 3) minimum solder mask web and minimum interconnect conductor width. The surface finish **shall** represent the product board design and the minimum web spacing and minimum conductor are per the product board. The design parameters for coupon G are shown in Table A.9-1.

Table A.9-1 G Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Rectangular lands	Grid size: 1.27 [0.050] Solder mask anti-land calculation: 1.27 [0.050] - minimum solder mask web Land calculation: Solder mask anti-land - (2 x minimum solder mask clip back)
2	Round lands	
C	Minimum conductor	Minimum interconnect conductor associated with the solder mask web features
SMOC	Solder mask over copper or surface finish	Solder mask anti-land size: 0.61 [0.024] Grid size: 0.64 [0.025]
SMOL	Solder mask over laminate	Solder mask anti-land size: 0.61 [0.024] Grid size: 0.64 [0.025]

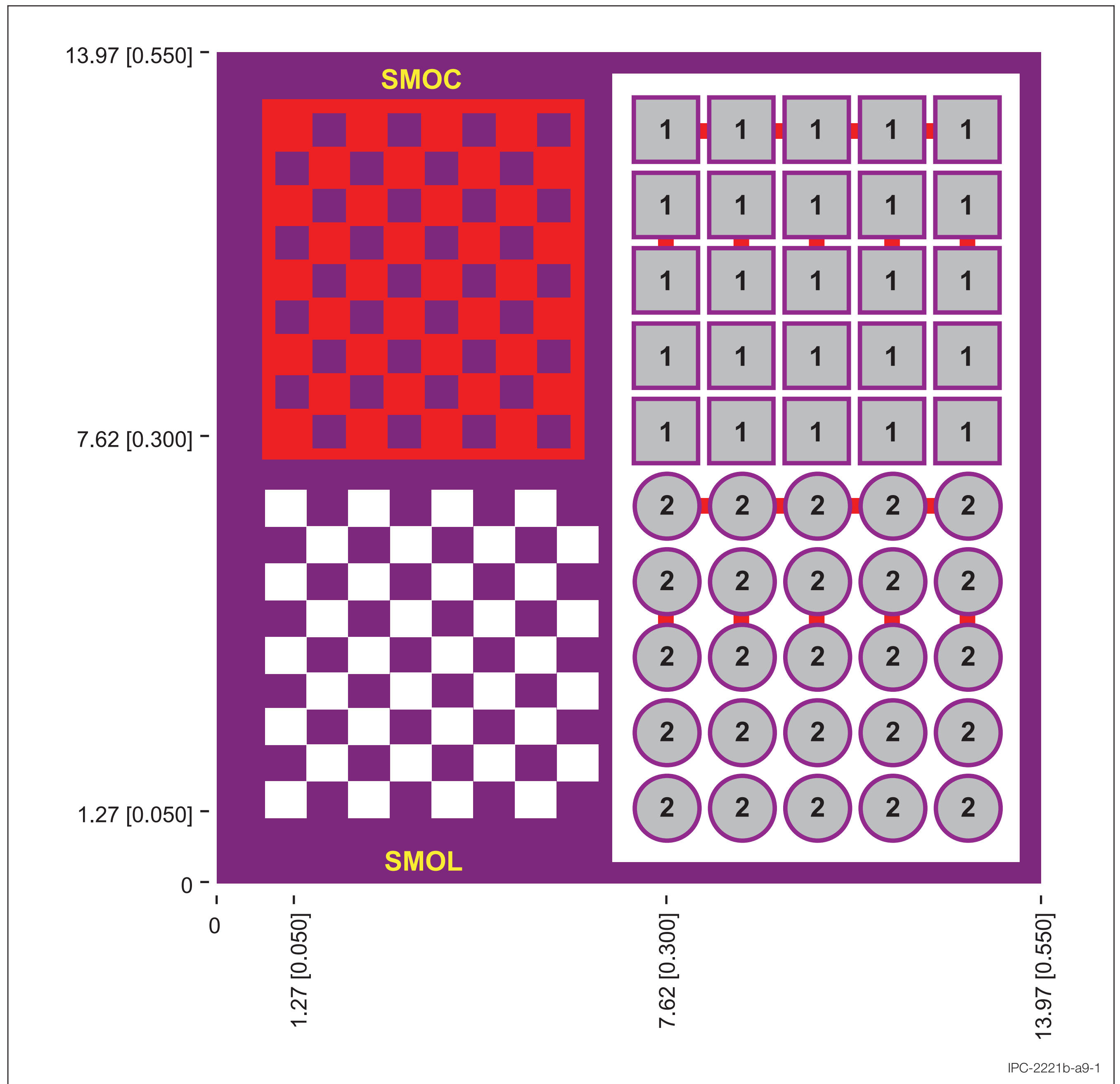

Figure A.9-1 G Coupon Layout, mm [in]

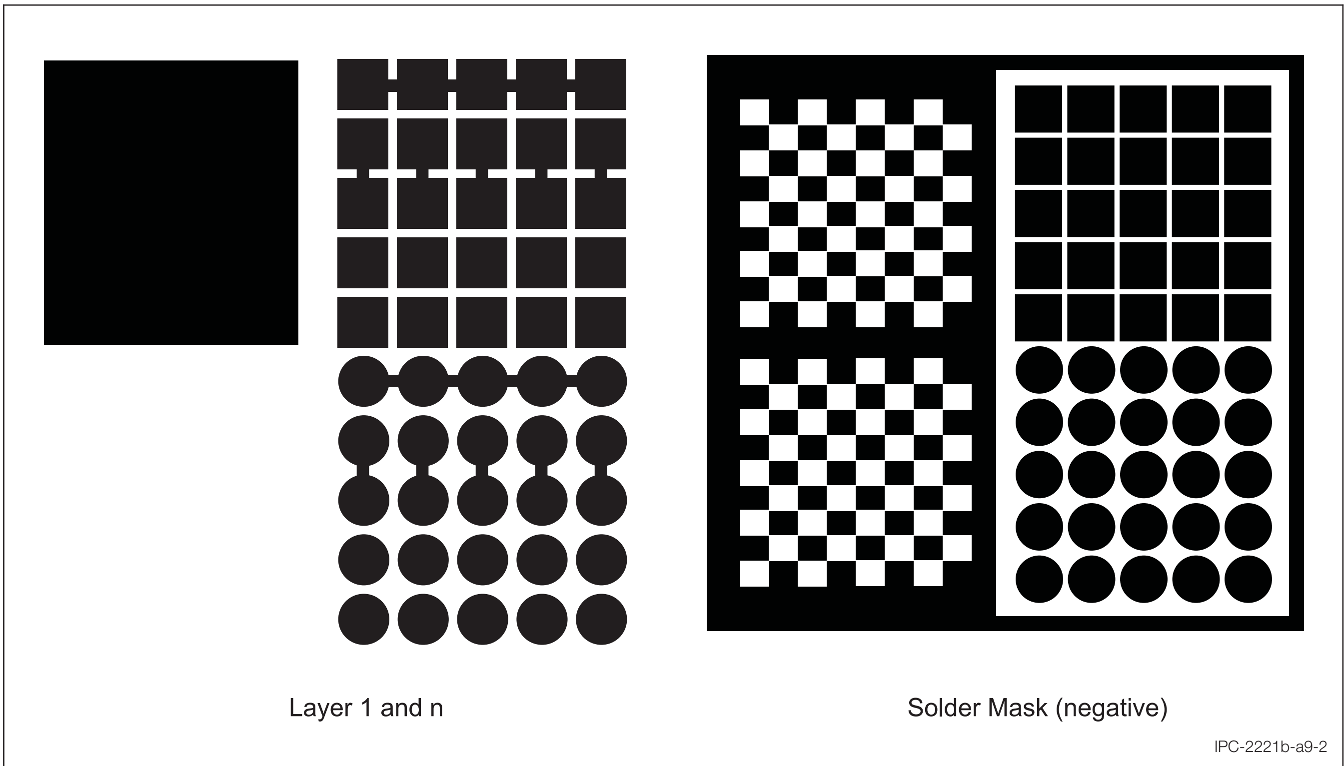

Figure A.9-2 G Coupon Example Layers

A.10 H COUPON Coupon H is used to quantify the effects of process and/or handling residues on surface insulation resistance. The coupon consists of an interstitial comb pattern per panel side. While a solder mask image is documented, the pertinent performance specification may preclude the use of solder mask on the coupon. The design parameters for coupon H are shown in Table A.10-1.

Table A.10-1 H Coupon Parameters, mm [in]

Feature	Description	Design Requirements
1	Plated-through test points	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060]
Electrodes	Parallel electrodes	Width: 0.40 [0.016] Pitch: 0.60 [0.024]

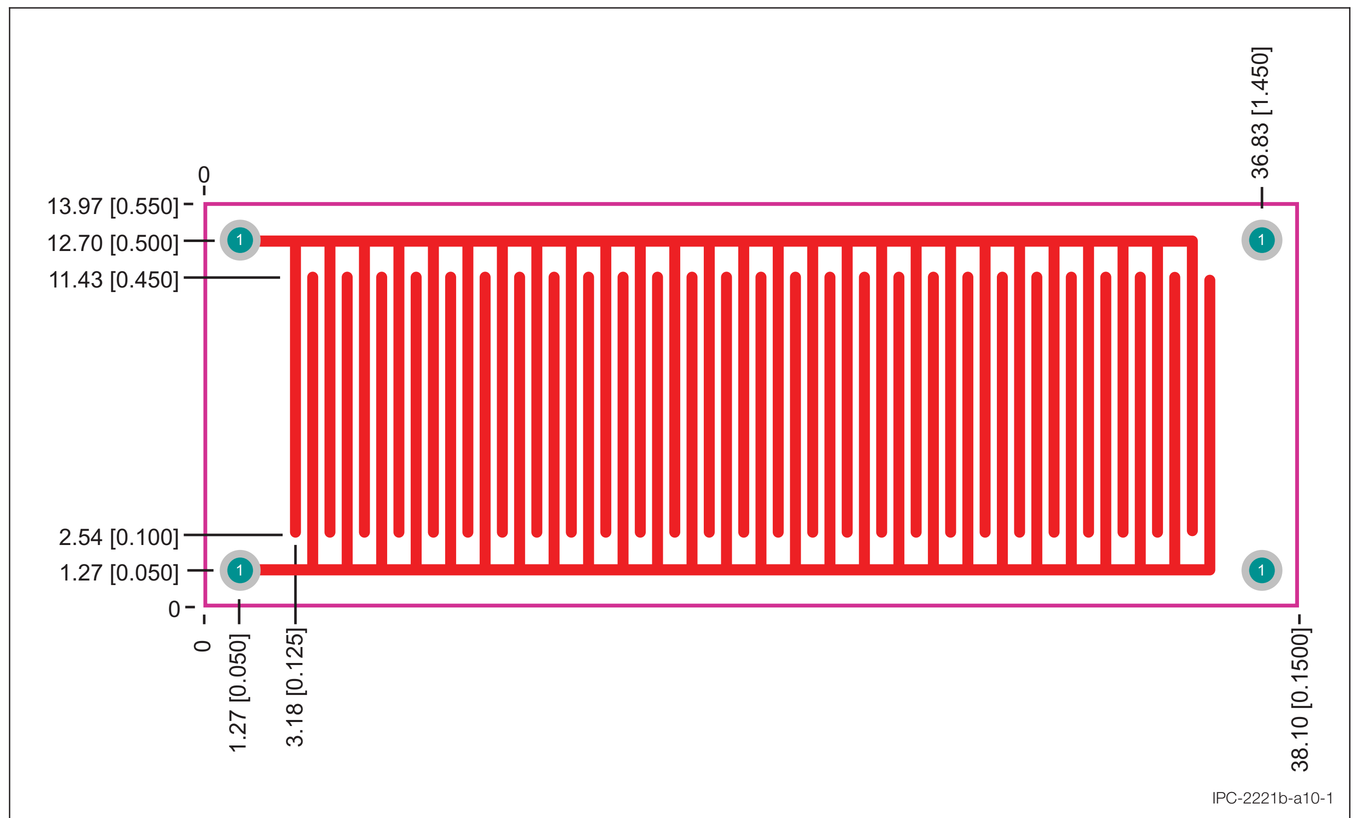

Figure A.10-1 H Coupon Layout, mm [in]

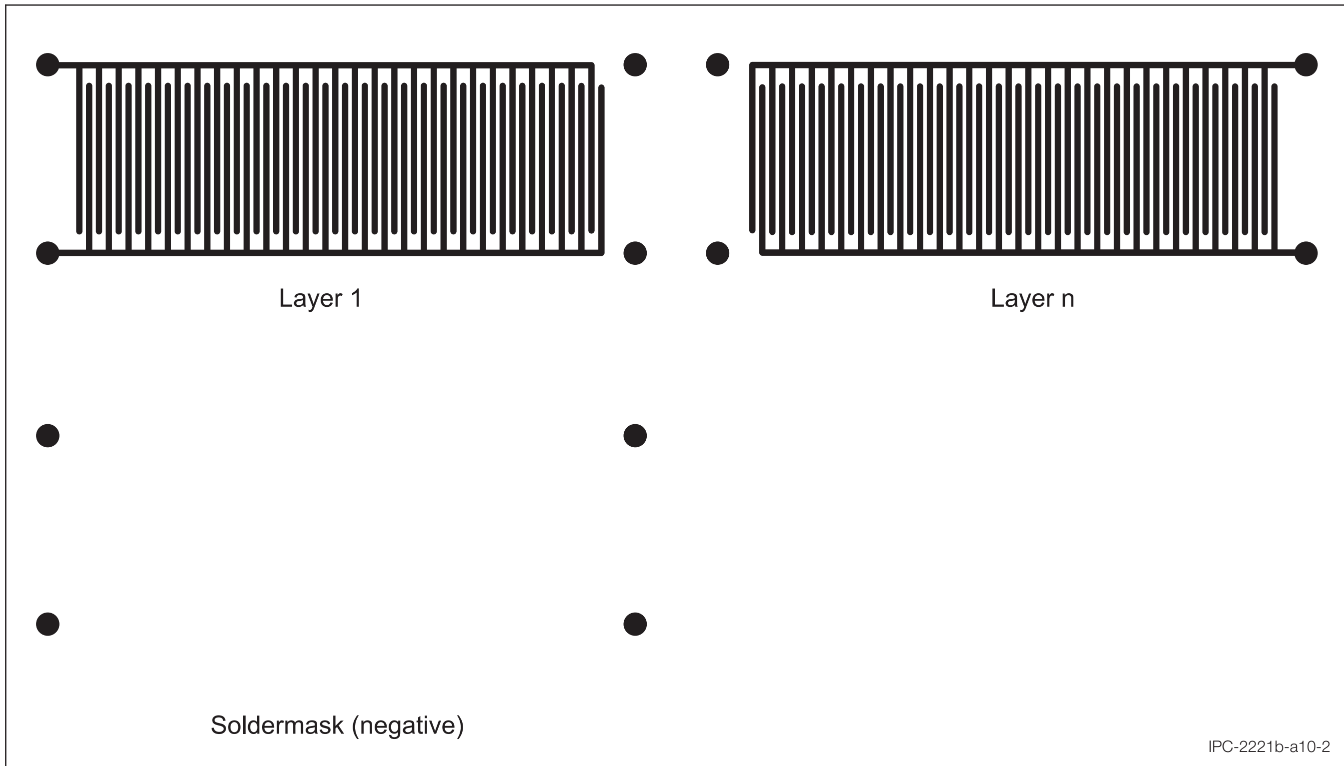

Figure A.10-2 H Coupon Example Layers

A.11 P COUPON Coupon P is used to evaluate the peel strength of metallic foils laminated to the outer layers of a printed board during the foil lamination process and to evaluate plating adhesion. The coupon consists of a conductor pair per panel side that provides a minimum test length of 30.48 [1.200]. The design parameters for coupon P are shown in Table A.11-1.

Table A.11-1 P Coupon Parameters, mm [in]

Feature	Description	Design Requirements
Peel	Peel conductor	Width: 3.18 [0.125] Minimum length: 30.48 [1.200]
Tab	Peel tab	Width: 5.72 [0.225] Length: 6.99 [0.275]

Note 1. Performance specifications preclude the use of surface finish on the coupon.

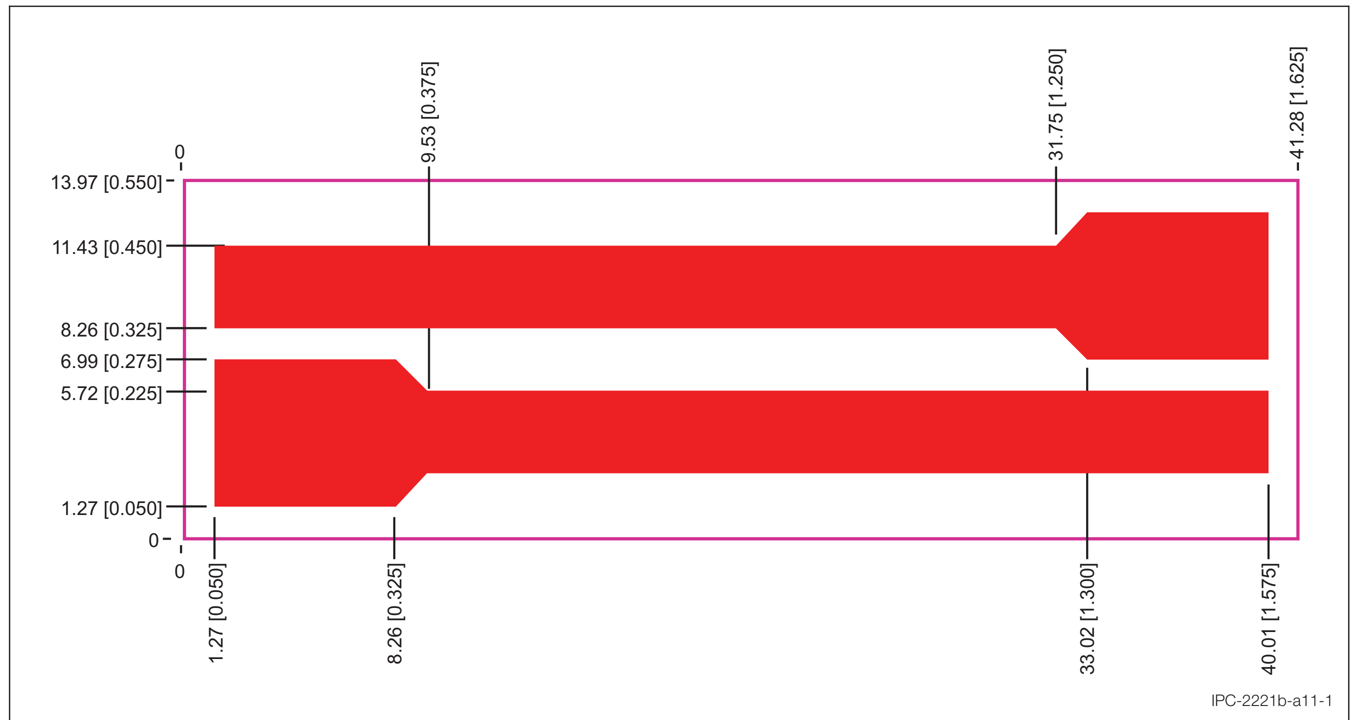

Figure A.11-1 P Coupon Layout, mm [in]

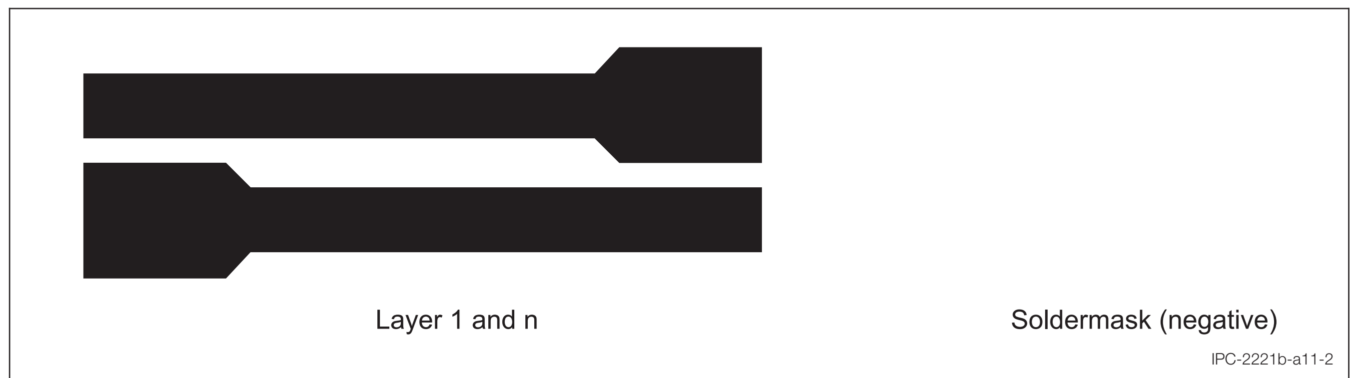

Figure A.11-2 P Coupon Example Layers

A.12 Z COUPON Coupon Z is used to determine the impedance value of controlled impedance structures of the printed board. Two structures either single-ended and/or differential per layer may be incorporated. The coupon may be designed with up to 24 single-ended structures, 12 differential structures or a combination of the two. The coupon provides for a minimum conductor length of 114.30 [4.50]. The design parameters for coupon Z are shown in Table A.12-1.

Table A.12-1 Z Coupon Parameters, mm [in]

Feature	Description	Design Requirements
TP	Plated-through test points (48 each)	Recommended drill size: 1.02 [0.040] Recommended land size: 1.52 [0.060] Grid size: 2.54 [0.100]
Conductors	Single-ended (2 test points): •Microstrip •Stripline Differential (4 test points): •Edge-coupled microstrip •Edge-coupled stripline •Broadside coupled stripline	Width(s): Per product board requirements Minimum length(s): 114.30 [4.50] Differential spacing: Per product board requirements Corners: Radiuses or 45 degree turns **Note:** Care should be taken to ensure constant separation of conductors on differential corners.
Planes	Reference planes	Edge of coupon clip-back: 0.254 [0.010] Spacing to edge of test-pad: 0.508 [0.020]

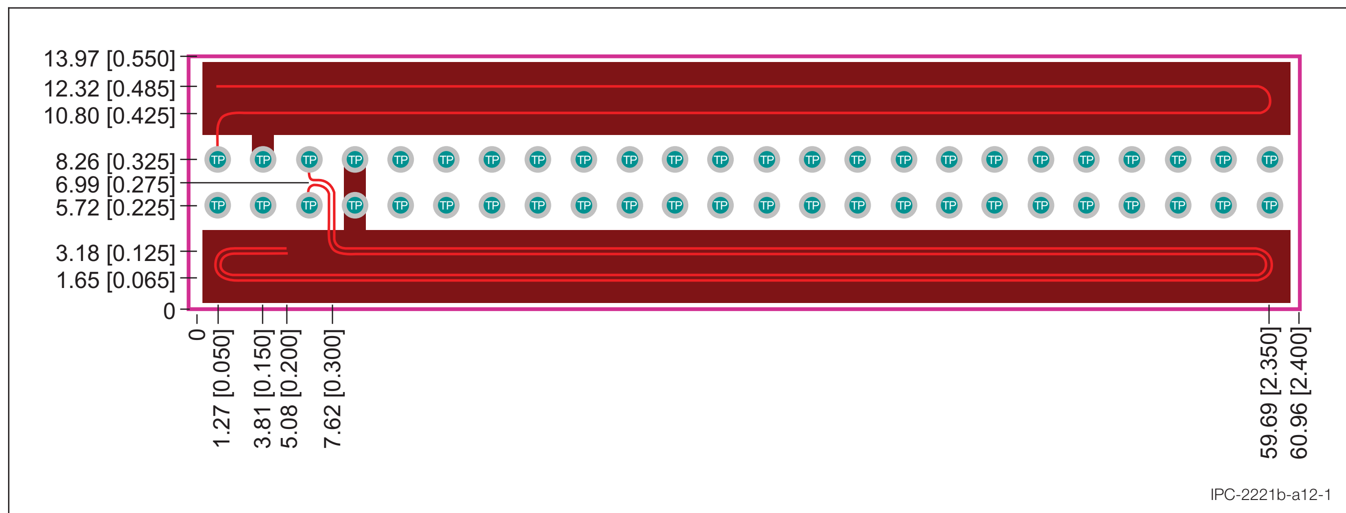

Figure A.12-1 Z Coupon Layout (Microstrip and edge-coupled microstrip), mm [in]

Signal Layer

Soldermask (negative)

Reference Plane Layer

IPC-2221b-a12-2

Figure A.12-2 Z Coupon Example Layers

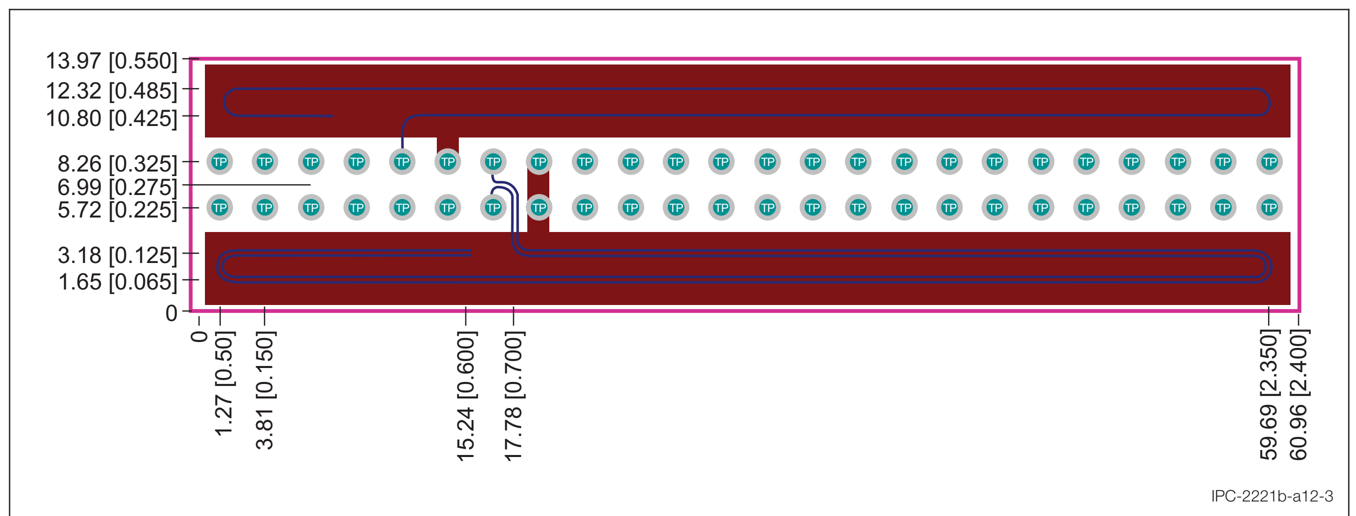

Figure A.12-3 Z Coupon Layout (Microstrip and edge-coupled microstrip using alternative test points), mm [in]